

REMARKS

Claims 1-10 and 14-21 are pending. Claims 1, 8 and 14 are amended. Claims 11-13 are canceled. Applicant requests reconsideration and reexamination of the pending claims.

Rejections under 35 U.S.C. 112, second paragraph:

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The Examiner has stated that in "independent claims 1, 11, and 14, it is unclear whether the processing temperature is that of the furnace or that of the wafer." The Examiner believes that the step of "keeping the temperature of furnace at steady-state processing temperature while removing the wafer from the chamber" is an omitted step. (Final Office Action dated May 21, 2003, p. 2)

Applicant argued in the Response to Non-Final Office Action dated February 6, 2003, that "if it is assumed that the wafer is at a processing temperature then the process chamber must also be at that temperature." Thus, Applicant was not silent on the issue of the temperature of the furnace. The internal environment of the furnace has been raised to a steady-state processing temperature which heats the wafer to the processing temperature. Thus, it follows that if the wafer has been raised to this temperature the chamber has also been raised to this temperature.

Applicant has amended Claim 1 to set forth "unloading the semiconductor wafer from said process chamber, while said internal environment of said process chamber remains at said steady-state processing temperature." Claim 14 has been amended to set forth "removing the at least one semiconductor wafer from said process chamber while said process chamber is kept at said steady-state temperature." Applicant submits that these features, in essence, are the same as what the Examiner has alleged is missing. Accordingly, there is no missing steps in Claims 1 and 14.

For the reasons above, Applicant requests that the rejections under 35 U.S.C. 112, second paragraph, be withdrawn.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 Michelson Drive
Suite 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Rejection under 35 U.S.C. 102

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolf, Silicon Processing for the VLSI Era, vol. 1-Process Technology: pp. 164-165, 169-178, 182-4, 194, and vol. 2-Process Integration: pp. 331, 431, 434-5. Applicant respectfully traverses the rejection as follows.

Claim 1 sets forth, *inter alia*, a method including "unloading the semiconductor wafer from said process chamber, while said internal environment of said process chamber remains at said steady-state processing temperature." Applicant could find no teaching or suggestion in Wolf that discloses the "unloading" feature of Claim 1.

The present invention includes unloading a semiconductor wafer from a process chamber at the same steady-state temperature as experienced during processing. In most processing applications, such as those described in the cited references, the processing temperature is reduced before the wafer is removed from the processing chamber, so that the cooling can facilitate the ending of the processing reactions that would otherwise continue to occur within the chamber.

Thus, although the Examiner has pointed to various descriptions in the cited references that allegedly show the method described in Claim 1, Applicant could find no teaching or suggestion in the cited references that would lead one of ordinary skill in the art to perform such a processing step. In Wolf, there is no teaching or suggestion that would lead one of ordinary skill in the art to consider removing the wafer from a processing chamber while the chamber is at a steady-state processing temperature.

In contrast, reactions that may occur in the process of Claim 1 can be ceased when the partial pressure of the reactive gas is adjusted "from said first partial pressure to a second partial pressure." Thus, in the present invention, it is possible to remove the wafer while the chamber is at steady-state processing temperature since no reaction is occurring that would adversely affect the wafer.

Applicants reiterate that Wolf provides disclosure regarding wafer processing in general, but fails to anticipate the method set forth in Claim 1.

Although, Applicant has amended Claim 1, it has been done only to clarify the method of the present invention and not to narrow Claim 1 in view of the cited references.

Accordingly, Claim 1 is allowable over the cited references.

Claims 11-13 are canceled.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 Michelson Drive
Suite 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Claim 14 sets forth a method including "removing the at least one semiconductor wafer from said process chamber while said process chamber is kept at said steady-state temperature." For reasons stated above with regard to Claim 1, Applicant could find no teaching or suggestion of such a feature in the cited references. Accordingly, Claim 14 is allowable over the cited references.

Claims 2-10 depend from Claim 1 and are therefore allowable for at least the same reasons as Claim 1. Claims 15-21 depend from Claim 14 and are therefore allowable for at least the same reasons as Claim 14.

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 Michelson Drive
Suite 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

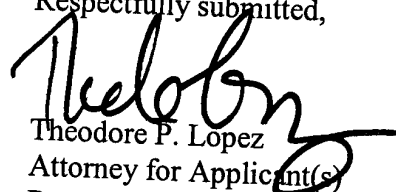
CONCLUSION

For the above reasons, pending Claims 1-10 and 14-21 are now in condition for allowance and allowance of the application is hereby solicited. If the Examiner has any questions or concerns, the Examiner is hereby requested to telephone Applicant's Attorney at (949) 752-7040.

Express Mail Label No.:

EV 252 520 015US

Respectfully submitted,


Theodore P. Lopez
Attorney for Applicant(s)
Reg. No. 44,881

LAW OFFICES OF
MACPHERSON KWOK CHEN
& HEID LLP

2402 Michelson Drive
Suite 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049